

Search Report

EIC 2800

STIC Database Tracking Number: 290930

To: JOSE DEES
Location: JEF-8D59
Art Unit: 2800
Monday, March 30, 2009

Patent Number: 6,297,140

From: DIANE JACKSON
Location: EIC2800
JEF-4B68
Phone: (571)272-3260

diane.jackson@uspto.gov

Search Notes

Attached are litigation search results in Lexis Nexis, and CourtLink and Questel-Orbit.

No Litigation was found for Patent Number 6,297,140.

If you have any questions, please feel free to contact me.

Thanks,

Diane

Jackson, Diane

MAR 30 2009

From: Dees, Jose

Sent: Friday, March 27, 2009 3:48 PM

To: STIC-EIC2800

Subject: Reissue 10/677166

Please do a litigation search for Patent No. 6,297,140.

Thanks, J Dees

Jose' G. Dees

Jose' G. Dees

TC-QAS, TC 2800

71-272-1569

Selected file: PLUSPAT

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& JPB
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Last update of file: 2009/03/27 (YYYY/MM/DD) 2009-13/UP (last update)

Search statement 1

nbr /pn us6297140

PLUSPAT1 US6297137	1
PLUSPAT2 US6297138	1
PLUSPAT3 US6297139	1
PLUSPAT4 US629714	1
PLUSPAT5 US6297140	1
PLUSPAT6 US6297141	1
PLUSPAT7 US6297142	1
PLUSPAT8 US6297143	1
PLUSPAT9 US6297144	1
PLUSPAT10US6297145	1
PLUSPAT11US6297146	1
PLUSPAT12US6297147	1
PLUSPAT13US6297148	1
PLUSPAT14US6297149	1
PLUSPAT15US629715	1

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** SS 1: Results 1

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☐ 1 / 1 PLUSPAT -
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US6297140 (B1) Method to plate C4 to copper stud
 PN US6297140 B1 20011002 [US6297140]
 TI (B1) Method to plate C4 to copper stud
 PA (B1) IBM (US)
 PA0 International Business Machines Corporation, Armonk NY [US]
 IN (B1) UZOH CYPRIAN EMEKA (US); EDELSTEIN DANIEL C (US)
 AP US38923299 19990903 [1999US-0389232]
 FD Divsn of US004808 19980109 [1998US-0004808]
 Division of: US6251528
 PR US38923299 19990903 [1999US-0389232]
 US480898 19980109 [1998US-0004808]
 IC (B1) H01L-021/44
 C25D-007/12 [2006-01 A F I R M JP]
 ICAA C23C-018/31 [2006-01 A L I R M JP]
 H01L-021/288 [2006-01 A L I R M JP]
 H01L-021/60 [2006-01 A - I R M EP]
 C25D-007/12 [2006 C F I R M JP]
 ICCA C23C-018/31 [2006 C L I R M JP]
 H01L-021/02 [2006 C - I R M EP]
 EC H01L-021/60B2
 ORIGINAL (O) : 438612000; CROSS-REFERENCE (X) : 257E21508
 PCL 438613000 438614000 438627000 438629000 438637000 438643000
 438653000 438674000 438675000 438676000 438677000 438678000
 438687000
 DT Corresponding document
 US4840302 [US4840302]
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 -US6080656 [US6080656] 438626000

-US6093647 [US6093647] 438687000
-US6140234 [US6140234] 438678000
-JP52-155055 [JP51155055]
-JP3-190240 A [JP03190240]

STG (B1) U.S. Patent (no pre-grant pub.) after Jan. 2, 2001

A method for plating a second metal directly to a first metal without utilizing a mask. A semiconductor substrate is provided including at least one metal feature and at least one insulating layer covering the metal feature and the substrate. At least one recess is formed in the at least one insulating layer thereby exposing at least a portion of the metal feature. At least one conductive barrier layer is formed over the insulating layer and the exposed portion of the metal feature. A plating seed layer of a first metal is formed over the at least one barrier layer. A photoresist layer is deposited over the plating seed layer. Portions of the photoresist layer and portions of the plating seed layer outside of the at least one recess are removed. Photoresist remaining in the at least one recess is removed. A second metal is electroplated to the plating seed layer in the recess, using the barrier layer to conduct electrical current.

UP 2001-41

Search statement 2

..fi fampat

Selected file: FAMPAT

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Abstracts/Titles in English , French & German. Increased
standardization

of Assignee/Inventor names. Added cited ref's BE , CH , NL , TR , AU , & JPB

For more details , see the FamPat Fact Sheet and Questel website

Last update of file: 2009/03/27 (YYYY/MM/DD) 2009-13/UP (last update)

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nbr /pn us6297140

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FAMPAT2 US6297138	1
FAMPAT3 US6297139	1
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FAMPAT12US6297147	1
FAMPAT13US6297148	1
FAMPAT14US6297149	1
FAMPAT15US629715	1

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Families - ©Questel

JP11274208 Method to plate C4 to copper stud

FAN 20042790907567

	JP11274208	A	19991008	[JP11274208]
	US6251528	B1	20010626	[US6251528]
PN	US6297140	B1	20011002	[US6297140]
	US2001032787	A1	20011025	[US20010032787]
	JP3245122	B2	20020107	[JP3245122]

TI Method to plate C4 to copper stud

PA IBM

PA0 International Business Machines Corporation, Armonk NY [US]

IN UZOH CYPRIAN EMEKA; EDELSTEIN DANIEL C

1998US-0004808 19980109

AP 1999JP-0003342 19990108

1999US-0389232 19990903

2001US-0887443 20010625

(US6297140)

FD Divsn of US004808 19980109 [1998US-0004808]

Division of: US6251528

(US20010032787)

FD Divsn. of: US 09004808 - 19980109 [1998US-0004808] GRANTED
Divsn. of: US 6251528 - 0 [US6251528]
1998US-0004808 19980109

PR 1999US-0389232 19990903
2001US-0887443 20010625
B32B-009/00
B32B-017/06
C23C-018/31
C25D-005/02

IC C25D-007/12
H01L-021/02
H01L-021/288
H01L-021/44
H01L-021/60
C25D-007/12 [2006-01 A F I R M JP]
C23C-018/31 [2006-01 A L I R M JP]

ICAA H01L-021/288 [2006-01 A L I R M JP]
H01L-021/60 [2006-01 A - I R M EP]
C25D-007/12 [2006 C F I R M JP]

ICCA C23C-018/31 [2006 C L I R M JP]
H01L-021/02 [2006 C - I R M EP]

EC H01L-021/60B2

PCL ORIGINAL (O) : 428587000; CROSS-REFERENCE (X) : 257E21508
428596000

FI C25D7/12; H01L21/288 E; H01L21/92 604H; H01L21/92 604R; C23C18/31
A
4K024 AA09; 4K024 AA22; 4K024 AB02; 4K024 AB03; 4K024 AB04;
4K024 AB08; 4K024 AB15; 4K024 AB17; 4K024 AB19; 4K024 BA07;
4K024 BB12; 4K024 BC10; 4K024 FA01; 4K024 FA05; 4K024 GA16;
4M104 BB04; 4M104 BB36; 4M104 CC01; 4M104 DD34; 4M104 DD38;
4M104 DD43; 4M104 DD52; 4M104 DD53; 4M104 EE06; 4M104 EE18;
4M104 FF06; 4M104 FF17; 4M104 FF18; 4K022 AA02; 4K022 DA01;
4K022 BA08; 4K022 AA05; 4K022 AA37; 4K022 AA41; 4K022 BA35;
4K022 CA28
(US6251528)
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-US5089440 [US5089440]
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CT -US5256274 [US5256274] 205123000
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-JP3-190240 A [JP03190240]
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-US6093647 [US6093647] 438687000
-US6140234 [US6140234] 438678000
-JP52-155055 [JP51155055]
-JP3-190240 A [JP03190240]
(JP11274208)

(A)

CT

[19] Citation as reason for refusal of an application
- JP (A) 1991190240 [JP03190240]
- JP (A) 1977155055 [JP52155055]
(US6251528)

AB

A method for plating a second metal directly to a first metal without utilizing a mask. A semiconductor substrate is provided including at least one metal feature and at least one insulating layer covering the metal feature and the substrate. At least one recess is formed in the at least one insulating layer thereby exposing at least a portion of the metal feature. At least one conductive barrier layer is formed over the insulating layer and the exposed portion of the metal feature. A plating seed layer of a first metal is formed over the at least one barrier layer. A photoresist layer is deposited over the

plating seed layer. Portions of the photoresist layer and of the plating seed layer outside of the at least one recess are removed. Photoresist remaining in the at least one recess is removed. A second metal is electroplated to the plating seed layer in the recess.

(US6251528)

The present invention relates to a process for plating a conductive material to a conductive feature in and/or on a substrate.

More particularly, the present invention concerns electroplating a conductive material to a metal feature in and/or on a substrate using a highly conducting barrier film to conduct electrical current.

OBJ In particular, the present invention provides methods for electroplating a solder ball utilized in a controlled collapse chip connection (C4) process to a metal feature provided in and/or on a substrate.

Additionally, the present invention provides semiconductor structures prepared according to processes of the present invention.

Broadly, an object of the present invention is to provide a process for selectively plating metal utilizing more than one metal as an electrode.

Aspects of the present invention also provide a method for plating a second metal directly to a first metal without utilizing a mask.

(US6251528)

One of the main advantages of the damascene process as compared to metal RIE is that it is often easier to etch an insulator as opposed to metal.

Also, insulator gap fill and planarization may be more problematic.

Another advantage of the present invention is that it may utilize a barrier metal to carry plating current.

A further advantage of the present invention is that it may eliminate plating of metal on pins.

ADB An additional advantage of the present invention is that it may provide higher productivity as compared to known processes.

In accordance with these and other objects and advantages, the present invention provides a method for plating a second metal directly to a first without utilizing a mask.

The present invention permits the second metal to be electroplated without utilizing a mask.

An advantage of the present invention is that it provides a less expensive process than known process for producing similar results.

Additionally, the process may be less costly as compared to typical lithographically defined C4 processes.

(US6251528)

1. A semiconductor structure, comprising:
a semiconductor substrate;

ICLM at least one metal feature provided in said substrate;

at least one insulating layer at least partially covering said at least one metal feature;

at least one recess located in said at least one insulating layer over said at least one metal feature;

at least one conductive barrier layer located over said at least one electrical insulating layer and over a portion of said at least one metal feature under said at least one recess, said conductive barrier layer comprising at least one nitride of tantalum and ALPHA -phase tantalum;
at least one plating seed layer of a first metal located over a portion of said conductive barrier layer within said at least one recess, said seed layer and barrier layer in combination forming a continuous conductive layer; and
a second metal electroplated to said seed layer within said at least one recess.

UP 2001-27

☐ 1 / 2 LGST - Legal 
Status - ©EPO

US6251528 20020409 US/CCA [COR]CERTIFICATE OF CORRECTION
PN US6251528 B1 20010626 [US6251528](B1) Granted patent as first publication
AP US480898 19980109 [1998US-0004808]
19980109 US-API [POS; EXM]
FILING DETAILS
US480898 19980109 [1998US-0004808]
PUB 20010626 US-B1 [POS; PIF]
Granted patent as first publication
US6251528 B1 20010626 [US6251528]
20020409 US/CC-A [COR]
ACT CERTIFICATE OF CORRECTION
COR
LEG Alive
UP 2003-22

☐ 2 / 2 LGST - Legal 
Status - ©EPO


US6297140 20020625 US/CCA [COR]CERTIFICATE OF CORRECTION
PN US6297140 B1 20011002 [US6297140](B1) Granted patent as first publication
AP US38923299 19990903 [1999US-0389232]
19990903 US-API [POS; EXM]
PUB FILING DETAILS
US38923299 19990903 [1999US-0389232]

20011002 US-B1 [POS; PIF]
Granted patent as first publication
US6297140 B1 20011002 [US6297140]
20020625 US/CC-A [COR]
CERTIFICATE OF CORRECTION

ACT 20040413 US/RF-A [OPP]
REISSUE APPLICATION FILED
EFFECTIVE DATE: 20031002

LEG OPP
Alive


UP 2004-17

☐ 1 / 2 CRXX - US Claims 
Reassignments - ©CLAIMS/RRX

US6297140 20031002 REISSUE REQUESTED
20040413 REISSUE REQUEST NUMBER...
AN 3582866
PN 6,297,140 A 20011002 [US6297140]
PA International Business Machines Corp
PT C (Chemical)
20031002 REISSUE REQUESTED
ISSUE DATE OF O.G.: 20040413
REISSUE REQUEST NUMBER: 10/677166
ACT EXAMINATION GROUP RESPONSIBLE FOR REISSUE PROCESS: 2812

Reissue Patent Number:

UP 2002-29
UACT 2004-04-13

☐ 2 / 2 CRXX - US Claims 
Reassignments - ©CLAIMS/RRX

US6251528 20020430 CERTIFICATE OF CORRECTION

AN 3532295
PN 6,251,528 A 20010626 [US6251528]
PA International Business Machines Corp
PT C (Chemical)
ACT 20020430 CERTIFICATE OF CORRECTION
UP 2002-18
UCOR 2002-04-30

Search statement 2

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389232 (09) 6297140 October 2, 2001

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

6297140[Get Drawing Sheet 1 of 2](#)[Access PDF of Official Patent *](#)[Order Patent File History / Wrapper from REEDFAX®](#)[Link to Claims Section](#)

October 2, 2001

Method to plate C4 to copper stud

INVENTOR: Uzoh, Cyprian Emeka - Hopewell Junction, New York, United States (US) Edelstein, Daniel C. - New Rochelle, New York, United States (US)

CERT-CORRECTION: June 25, 2002 - a Certificate of Correction was issued for this patent (O.G. July 16, 2002)

APPL-NO: 389232 (09)**FILED-DATE:** September 3, 1999**GRANTED-DATE:** October 2, 2001

ASSIGNEE-PRE-ISSUE: September 3, 1999 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., INTERNATIONAL BUSINESS MACHINES CORPORATION OLD ORCHARD ROAD ARMONK, NEW YORK, 10504, Reel and Frame Number: 010421/0816

ASSIGNEE-AT-ISSUE: International Business Machines Corporation, Armonk, New York, United States (US), United States company or corporation (02)

LEGAL-REP: Connolly Bove Lodge & Hutz Abate, Joseph P.

PUB-TYPE: October 2, 2001 - Utility Patent having no previously published pre-grant publication (B1)

PUB-COUNTRY: United States (US)

REL-DATA:

Division of Ser. No. 09/004808, January 9, 1998, GRANTED PATENT 6251528, Utility Patent having no previously published pre-grant publication (A)

US-MAIN-CL: 438#612

US-ADDL-CL: 257#E21.508, 438#613, 438#614, 438#627, 438#629, 438#637, 438#643, 438#653, 438#674, 438#675, 438#676, 438#677, 438#678, 438#687

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